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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER

CHEN, TSE W

ART UNIT

PAPER NUMBER

2116

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/964,010

Applicant(s)

HAYCOCK ET AL.

Examiner

Tse Chen

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) 1-9 and 23-30 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10-13, 15 and 18-22 is/are rejected.
- 7) ☒ Claim(s) 14, 16 and 17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 September 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) • | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated August 26, 2004.
2. Applicant has elected claims 10-17 and 18-22 for examination. Applicant has canceled claims 1-9 and 23-30.

Claim Objections

3. Claim 15 is objected to because of the following informalities: "logic function" should be "logic circuit" in order to comply with established antecedent in claim 10. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Re Claim 10

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taya et al., US Patent 5778214, hereinafter Taya, in view of Yamamoto et al., Japanese Publication 06-120937, hereinafter Yamamoto.
6. Taya discloses an integrated circuit [pattern detection circuit 2] comprising:
 - A plurality of input nodes [delay elements] to receive a plurality of input bits [fig.2; inputs to the registers].

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- A plurality of output nodes [sync pattern check circuits] to provide a plurality of output bits [fig.2; outputs from check circuits].
 - A plurality of register circuits [shift registers], each of the register circuits being connected between one of the input nodes and one of the output nodes [fig.2; between the delay elements and the check circuits].
7. Taya did not discuss the details of a logic circuit or controller.
8. Yamamoto discloses an integrated circuit [abstract, accompanying figure] comprising:
- A logic circuit [comparison means 3] connected to the register circuits [shift registers] to perform a logic function [compare] on a plurality of bits held by the register circuits [paragraph 0011].
 - A controller [control means 5] to configure the register circuits based on a result from the logic circuit to align the plurality of output bits provided by one output node [output from shift register 1] with a plurality of output bits provided by other output nodes [output from shift register 2] when the plurality of input bits received at the input nodes [inputs to the shift registers] are misaligned by one or more bit time intervals [paragraphs 0012-0013].
9. It would have been obvious to one of ordinary skill in the art, having the teachings of Taya and Yamamoto before him at the time the invention was made, to modify the system taught by Taya to include the logic circuit and controller taught by Yamamoto, in order to obtain the claimed integrated circuit with simplicity and reduction in current consumption [Yamamoto: abstract]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to synchronize with simplicity and reduction in current consumption.

Re Claim 11

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taya and Yamamoto as applied to claim 10 above, and further in view of Fukuoka, US Patent 6467063.

11. Taya and Yamamoto disclose each an every limitation of the claim as discussed above in reference to claim 10. Taya and Yamamoto did not discuss the details regarding the number of register cells as related to the maximum number of bit timer intervals of misalignment.

12. Fukuoka discloses a circuit [Reed Solomon coding apparatus] comprising:

- Register circuits [90-97] that include a number of register cells, wherein the number of register cells equals $2M-1$ [$2s-1$], where M [s] is a maximum number of bit time intervals of misalignment [maximum number of errors] [col.14, ll.48-60].

13. It would have been obvious to one of ordinary skill in the art, having the teachings of Fukuoka, Taya and Yamamoto before him at the time the invention was made, to modify the system taught by Taya and Yamamoto to include the register circuits taught by Fukuoka, in order to obtain the claimed integrated circuit wherein each of the register circuits includes a number of register cells, wherein the number of register cells equals $2M-1$, where M is a maximum number of bits time intervals of misalignment of a parallel bus that connects to the integrated circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to correct multiple errors in a processing system [Fukuoka: col.1, ll.6-15].

Re Claims 12-13

14. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuoka, Taya and Yamamoto as applied to claim 11 above, and further in view of Moriwaki et al., US Patent 6753872, hereinafter Moriwaki.

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15. In re claim 12, Fukuoka, Taya and Yamamoto disclose each an every limitation of the claim as discussed above in reference to claim 11. Fukuoka, Taya and Yamamoto did not discuss the details of a select circuit.

16. Moriwaki discloses a system [rendering processing system] comprising register circuits that include:

- A select circuit [selector 51] connected to a subset of the number of register cells [set of 50-x registers] through a number of select lines [24b] [fig.5; col.9, ll.7-54].

17. It would have been obvious to one of ordinary skill in the art, having the teachings of Moriwaki, Fukuoka, Taya and Yamamoto before him at the time the invention was made, to modify the system taught by Fukuoka, Taya and Yamamoto to include the select circuit taught by Moriwaki, in order to obtain the claimed integrated circuit wherein each of the register circuits further includes a select circuit connected to a subset of the number of register cells through a number of select lines. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to select and process particular sets of data bits [Moriwaki: col.9, ll.24-42].

18. As to claim 13, Moriwaki, Fukuoka, Taya and Yamamoto discloses each an every limitation of the claim as discussed above in reference to claim 12. It would have been obvious to one of ordinary skill in the art, having the teachings of Moriwaki, Fukuoka, Taya and Yamamoto before him at the time the invention was made, to modify the system taught by Fukuoka, Taya and Yamamoto to include the select lines taught by Moriwaki, in order to obtain the claimed integrated circuit wherein the number of select lines equals a maximum number bit time intervals of misalignment of a parallel bus that connects to the integrated circuit. One of

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ordinary skill in the art would have been motivated to make such a combination as it provides a way to select and process particular sets of data bits [Moriwaki: col.9, ll.24-42; associate select lines with M since there's no need to further process bits greater than the maximum error].

Re Claim 15

19. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taya and Yamamoto as applied to claim 10 above, and further in view of Jaquette, US Patent 5737371.

20. Taya and Yamamoto disclose each an every limitation of the claim as discussed above in reference to claim 10. Taya and Yamamoto did not discuss the details of the logic circuit.

21. Jaquette discloses a logic circuit that performs an OR function [col.5, 1.54 – col.7, 1.15].

22. It would have been obvious to one of ordinary skill in the art, having the teachings of Jaquette, Taya and Yamamoto before him at the time the invention was made, to use the logic circuit with the OR function taught by Jaquette for the integrated circuit disclosed by Taya and Yamamoto as the logic circuit with the OR function taught by Jaquette is a very well known function suitable for use with the integrated circuit of Taya and Yamamoto. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to validate certain conditions with a well-known logic function [Jaquette: col.5, 1.54 – col.6, 1.9].

Re Claims 18-20

23. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki in view of Grondalski, US Patent 6108763.

24. In re claim 18, Moriwaki discloses a system [rendering processing system] comprising:

- A parallel bus [internal data bus 15] including a plurality of bus lines to carry a plurality of bits on each of the bus lines [fig.5; col.9, ll.7-23].

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- A first integrated circuit [data transfer circuit 12] including a plurality of register circuits [50-1 to 50-64], each of the register circuits being connected to one of the bus lines [col.9, ll.7-23].
- Each of the register circuits including:
 - A register [set of three 24-bits 50-x registers combined for 64 bits] connected to an input node [inherently, an input node in the broadest interpretation is at the other end of the bus], the register including a plurality of register cells [set of 50-x registers] [col.9, ll.7-41].
 - A select circuit [selector 51] connected to a subset of the number of register cells through a number of select lines [24b], the select circuit including an output node [switch circuit 52] [fig.5; col.9, ll.24-54].
 - A controller [memory control circuit 4] connected to the select circuit and the register cells to configure the register cells to select the select lines to be a part of a conductive path connected between the input node and the select circuit output node [col.9, l.24 – col.10, l.17; selector selects the 64 bits to be connected].

25. Moriwaki did not disclose explicitly that the registers are to be shift registers or that only one of the select lines is to be selected.

26. Grondalski discloses a system [fig.4] comprising:

- A shift register [52] including a plurality of register cells [col.19, ll.40-54].
- A controller [issues the sel cell signal] connected to the register cells to configure the register cells to select only one of the select lines [col.21, ll.12-56; sel cell signal corresponding to sel8 with associated transistors for particular register cell].

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27. It would have been obvious to one of ordinary skill in the art, having the teachings of Moriwaki and Grondalski before him at the time the invention was made, to use the shift register taught by Grondalski for the system disclosed by Moriwaki as the shift register taught by Grondalski is a well known device suitable for use as the register of Moriwaki. One of ordinary skill in the art would have been motivated to make such a combination as it provides a well-known way to manipulate data in a processing system [Grondalski: col.19, 1.40 – col.20, 1.22].

28. As to claim 19, Moriwaki discloses the system comprising a second integrated circuit [rendering operation circuit 2] connected to the parallel bus [fig.5].

29. As to claim 20, Moriwaki discloses the system wherein the parallel bus is formed on a circuit board, and the first and second integrated circuits are located in the circuit board [col.6, 1.64 – col.7, 1.22; on board wiring of bus].

Re Claim 21

30. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki and Grondalski as applied to claim 19 above, and further in view of Barnsley et al., US Patent 5430812, hereinafter Barnsley.

31. Moriwaki and Grondalski disclose each an every limitation of the claim as discussed above in reference to claim 19. Moriwaki and Grondalski did not discuss separate circuit board configuration.

32. Barnsley discloses a system [fig.5; digital image data compression apparatus] comprising:

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- A first circuit board [pc 112], wherein the parallel bus [AT bus 118] is formed on the first circuit board and a first integrated circuit [80386] is located on the first circuit board [col.4, ll.53-68].
- A second circuit board [110], wherein a second integrated circuit [fractal transform chips] is located on the second circuit board, the second circuit board being inserted into a bus slot that connects to the parallel bus [col.4, ll.53-68].

33. It would have been obvious to one of ordinary skill in the art, having the teachings of Barnsley, Moriwaki and Grondalski before him at the time the invention was made, to use the circuit board configuration taught by Barnsley for the system disclosed by Moriwaki and Grondalski as the circuit board configuration taught by Barnsley is a well known configuration suitable for use with the system of Moriwaki and Grondalski. One of ordinary skill in the art would have been motivated to make such a combination as it provides a well-known way to interconnect various parts in a processing system [Barnsley: col.4, ll.53-68].

Re Claim 22

34. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki and Grondalski as applied to claim 19 above, and further in view of Frisch et al., US Patent 4707834, hereinafter Frisch.

35. Moriwaki and Grondalski disclose each an every limitation of the claim as discussed above in reference to claim 19. Moriwaki and Grondalski did not discuss separate circuit board configuration.

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36. Frisch discloses a system [instrument system] comprising a first and second integrated circuit [instruments 12] that are located on separate circuit boards, and the parallel bus [26] is not formed on the first or second circuit boards [col.4, ll.28-58].

37. It would have been obvious to one of ordinary skill in the art, having the teachings of Frisch, Moriwaki and Grondalski before him at the time the invention was made, to use the circuit board configuration taught by Frisch for the system disclosed by Moriwaki and Grondalski as the circuit board configuration taught by Frisch is a well known configuration suitable for use with the system of Moriwaki and Grondalski. One of ordinary skill in the art would have been motivated to make such a combination as it provides a well-known way to interconnect various parts in a processing system [Frisch: col.4, ll.28-58].

Allowable Subject Matter

38. Claims 14 and 16-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

39. The following is a statement of reasons for the indication of allowable subject matter: the claims are allowable because none of the references cited, either alone or in combination discloses or renders obvious an integrated circuit with the limitations of claim 14 and the associated base claim and the intervening claims.

Conclusion

40. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited U.S. patent documents describe various methods for synchronizing and aligning data bits.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
October 19, 2004


LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 3600 2100